MSP430FR573x, MSP430FR572x Device Erratasheet

1 Current Version

See Appendix A for prior silicon revisions.

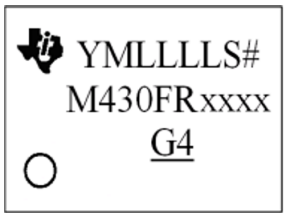
✓ The checkmark means that the issue is present in the specified revision.

Device	Rev:	CPU40	EEM19	MPY1	PORT16
MSP430FR5720	H	✓	✓	✓	✓
MSP430FR5721	H	✓	✓	✓	✓
MSP430FR5722	H	✓	✓	✓	✓
MSP430FR5723	H	✓	✓	✓	✓
MSP430FR5724	H	✓	✓	✓	✓
MSP430FR5725	H	✓	✓	✓	✓
MSP430FR5726	H	✓	✓	✓	✓
MSP430FR5727	H	✓	✓	✓	✓
MSP430FR5728	H	✓	✓	✓	✓
MSP430FR5729	H	✓	✓	✓	✓
MSP430FR5730	H	✓	✓	✓	✓
MSP430FR5731	H	✓	✓	✓	✓
MSP430FR5732	H	✓	✓	✓	✓
MSP430FR5733	H	✓	✓	✓	✓
MSP430FR5734	H	✓	✓	✓	✓
MSP430FR5735	H	✓	✓	✓	✓
MSP430FR5736	H	✓	✓	✓	✓
MSP430FR5737	H	✓	✓	✓	✓
MSP430FR5738	H	✓	✓	✓	✓
MSP430FR5739	H	✓	✓	✓	✓

2 Package Markings

DA38

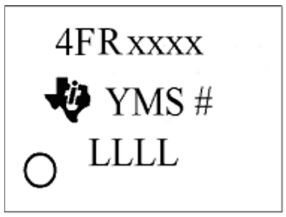
TSSOP (DA), 38 Pin



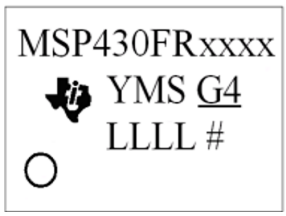
YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

PW28

TSSOP (PW), 28 Pin



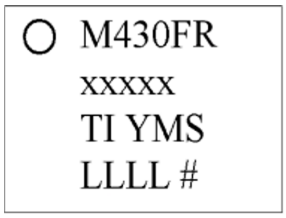
YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RGE24

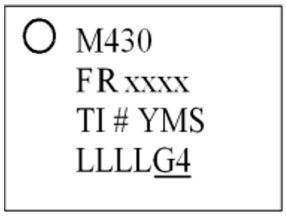
QFN (RGE), 24 Pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

RHA40

QFN (RHA), 40 Pin



YM = Year and Month Date Code
LLLL = LOT Trace Code
S = Assembly Site Code
# = DIE Revision
o = PIN 1

3 Detailed Bug Description

CPU40 *CPU Module*

Function

PC is corrupted when executing jump/conditional jump instruction that is followed by instruction with PC as destination register or a data section

Description

If the value at the memory location immediately following a jump/conditional jump instruction is 0X40h or 0X50h (where X = don't care), which could either be an instruction opcode (for instructions like RRCM, RRAM, RLAM, RRUM) with PC as destination register or a data section (const data in flash memory or data variable in RAM), then the PC value is auto-incremented by 2 after the jump instruction is executed; therefore, branching to a wrong address location in code and leading to wrong program execution.

For example, a conditional jump instruction followed by data section (0140h).

```
@0x8012  Loop    DEC.W R6
@0x8014          DEC.W R7
@0x8016          JNZ Loop
@0x8018  Value1  DW 0140h
```

Workaround

In assembly, insert a NOP between the jump/conditional jump instruction and program code with instruction that contains PC as destination register or the data section.

EEM19 *Enhanced Emulation Module*

Function

DMA may corrupt data in debug mode

Description

When the DMA is enabled and the device is in debug mode, the data transferred by the DMA may be corrupted when a breakpoint is hit or when the debug session is halted.

NOTE: This erratum applies to debug mode only.

Workaround

None. Do not set a breakpoint during a DMA transfer.

MPY1 *Hardware Multiplier (MPY) Module*

Function

Save and Restore feature on MPY32 not functional

Description

The MPY32 module uses the Save and Restore method which involves saving the multiplier state by pushing the MPY configuration/operand values to the stack before using the multiplier inside an Interrupt Service Routine (ISR) and then restoring the state by popping the configuration/operand values back to the MPY registers at the end of the ISR. However due to the erratum the Save and Restore operation fails causing the write operation to the OP2H register right after the restore operation to be ignored as it is not preceded by a write to OP2L register resulting in an invalid multiply operation.

Workaround

None. Disable interrupts when writing to OP2L and OP2H registers.

NOTE: When using the C-compiler, the interrupts are automatically disabled while using the MPY32.

PORT16 *Digital I/O Module*

Function

GPIO pins are driven low during device start-up

Description

During device start-up, all of the GPIO pins are expected to be in the floating input state. Due to this erratum, some of the GPIO pins are driven low for the duration of boot code execution during device start-up, if an external reset event (via the $\overline{\text{RST}}$ pin) interrupted the previous boot code execution. Boot code is always executed after a BOR, and the duration of this boot code execution is approximately 500 µs.

For a given device family, this erratum affects only the GPIO pins that are not available in the smallest package device family member, but that are present on its larger package variants.

NOTE: This erratum does not affect the smallest package device variants in a particular device family.

Workaround

Ensure that no external reset is applied via the $\overline{\text{RST}}$ pin during boot code execution of the device, which occurs 1 µs after device start-up.

NOTE: System application needs to account for this erratum to ensure that there is no increased current draw by the external components or damage to the external components in the system during device start-up.

Appendix A Prior Versions

✓ The checkmark means that the issue is present in the specified revision.

Device	Rev:	CPU40	EEM19	MPY1	PORT16
MSP430FR5720	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5721	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5722	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5723	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5724	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5725	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5726	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5727	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5728	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5729	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5730	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5731	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5732	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5733	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓

Device	Rev:	CPU40	EEM19	MPY1	PORT16
MSP430FR5734	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5735	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5736	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5737	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5738	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓
MSP430FR5739	F	✓	✓	✓	✓
	G	✓	✓	✓	✓
	H	✓	✓	✓	✓

Revision History

Changes from A Revision (October 2011) to B Revision	Page
• Added silicon revisions G and H	1

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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